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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/865,006	05/23/2001	Krishna Parat	042390P7462D	4672

7590 08/24/2004
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EXAMINER

DIAZ, JOSE R

ART UNIT	PAPER NUMBER
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2815

DATE MAILED: 08/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/865,006

Applicant(s)

PARAT ET AL.

Examiner

José R. Díaz

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 17 July 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 4-14 is/are pending in the application.
- 4a) Of the above claim(s) 12-14 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 4-11 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Election/Restrictions

1. Newly submitted claims 12-14 are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons: the process as claimed can be used to make other and materially different product. In the instant case, a semiconductor device comprising a trench structure with flat corners. Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 12-14 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Claim Objections

2. Claim 6 is objected to because of the following informalities:

the step "etching said second polysilicon...and said planarized second polysilicon" should be changed to --etching said first polysilicon...and said planarized second polysilicon"---.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

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A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claim 4 is rejected under 35 U.S.C. 102(e) as being anticipated by Witek et al. (US Pat. No. 6,146,970), previously cited.

Regarding claim 4, Witek et al. teaches a method comprising:

forming a trench (310) in a silicon substrate (302) (see fig. 15);

growing an oxide (312) in said trench (see fig. 16);

removing said grown oxide (312) in said trench (please note that oxide 312, although not shown, is removed from the top sidewall portions of the trench 310. See fig. 18);

growing a second oxide (317) in said trench (see fig. 19 and col. 9, lines 66-67);

filling said trench with a dielectric (318a) (see fig. 20);

growing a tunnel oxide (352) on said silicon substrate adjacent to said dielectric filled trench (see fig. 22);

forming a first polysilicon layer (366) on said tunnel oxide [see fig. 22 and col. 8, line 66 (e.g. "gate polysilicon stack")];

forming an interpoly dielectric (368) on said first polysilicon layer (see fig. 22);

forming a polysilicon control gate (370) on said interpoly dielectric [see fig. 22 and col. 9, lines 25-26 (e.g. "control gate polysilicon layer")].

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5. Claims 5 and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Sung et al. (US Pat. No. 5,734,607).

Regarding claim 5, Sung et al. teaches a method comprising:

forming a first and a second polysilicon/dielectric/polysilicon stack [consider polysilicon 12 (col. 3, lines 63-64), dielectric 13 (col. 4, lines 7-11), and polysilicon 14 (col. 4, lines 4-5)] on a tunnel oxide [consider oxide 9 (col. 3, lines 55-56)] of a substrate (11) (see fig. 1A), wherein said first and second stacks are separated by a gap (22') (see figs. 2C and 2I);

forming a shared source region (27) in said gap between said first and said second polysilicon/dielectric/polysilicon stacks (see fig. 2C);

forming a first drain region (26) adjacent to said first stack on the side opposite said shared source region (see fig. 2C);

forming a second drain region (26) adjacent to said second stack on the side opposite said shared source region (see fig. 2C);

forming a dielectric layer (29) over said first and said second stacks and over said first and said second drains wherein said dielectric layer completely fills said gap (22') between said shared source region (see figs. 2E and 2I) ;

anisotropically etching¹ said dielectric layer (29) from said first drain region and said second drain region (26) so as to form a first spacer on the side of said first stack adjacent to said first drain and to form a second spacer on the side of said second stack

¹ Please consider column 6, lines 57-59 in which Sung et al. teaches a dry, "plasma etching with a gas of SF₆", which inherently results in an *anisotropic* etch process. See Streetman et al., "Solid State Electronic Devices", 5th Ed., Prentice Hall, 2000, pages 155-156. Specifically, section 5.1.7, lines 8-10, wherein Streetman et al. states "dry, plasma-based etching which can be made both selective and *anisotropic*."

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adjacent to said second drain (consider portions 29') wherein in after said anisotropic etch steps said gap (22') remains filled with dielectric (consider portion 29") (see fig. 2F and 2I).

Regarding claim 8, Sung et al. teaches a trench (22') in a dielectric material (15) to the gap (see fig. 2I).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. (US 2001/0012661 A1) in view of Chi et al. (US Pat. No. 6,184,084 B1).

Regarding claim 6, Lin et al. teaches a method comprising:

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forming a tunnel oxide (31) on a substrate (21) (see fig. 3);
forming and patterning a first polysilicon film (32) on said tunnel oxide (see fig. 5);
forming a interpoly dielectric (51) on said patterned first polysilicon film (see fig. 6);
forming a second polysilicon film (61) over said interpoly dielectric over said first patterned polysilicon film (see fig. 7); and
etching said first polysilicon film (32), said interpoly dielectric (51), and said second polysilicon film (61) to form a polysilicon/dielectric/polysilicon stack having a planar top surface (consider the top planar surface of the polysilicon 61) (see fig. 8).

However, Lin et al. fails to teach the limitation of polishing said second polysilicon film to form a second polysilicon film with a substantially planar top surface. Chi et al. teaches that it is well known in the art to polish the second polysilicon film (48) to form a second polysilicon film with a substantially planar top surface (see col. 7, lines 26-30).

Lin et al. and Chi et al. are analogous art because they are from the same field of endeavor as applicant's invention. At the time of the invention it would have been obvious to a person of ordinary skill in the art to polish the second polysilicon film to form a second polysilicon film with a substantially planar top surface. The motivation for doing so, as is taught by Chi et al., is decreasing cracking of the poly 2 layer (col. 3, lines 14-21). Therefore, it would have been obvious to combine Chi et al. with Lin et al. to obtain the invention of claim 6.

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9. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wang (US Pat. No. 5,597,751).

Regarding claim 7, Wang teaches a method comprising the step of:

forming a first and a second polysilicon/dielectric/polysilicon stacks [consider polysilicon 44 (fig. 2), dielectric ("ONO spacer") (col. 4, lines 20-22), and polysilicon 48 (fig. 2)] on a tunnel oxide [consider oxide 42 (col. 4, line 18)] formed on a substrate (34) (see fig. 2), wherein said first and second stacks are separated by a gap (consider the space between adjacent stacks. See fig. 2);

forming a shared source region (36) in said silicon substrate in said gap (see fig. 2);

forming a first drain region (62) adjacent to said first stack opposite said shared source region (see figure 6), and a second drain region (62) adjacent to said second stack opposite said shared source (see figure 6);

forming a dielectric layer (50) over first and second portions of the substrate in which the drain regions (62) are formed, over said first stack over said shared source, and over said second stack (see fig. 2);

anisotropically etching (see col. 4, lines 49-50) said dielectric layer (50) to form spacer (54) adjacent to said first stack and on said first portion of the substrate in which the drain region (62) is formed; and a second spacer (54) adjacent to said second stack and on said second portion of the substrate in which the drain region (62) is formed (see fig. 4);

forming a metal film over said drain regions (62), said spacers (54), and said stacks (see col. 4, lines 62-64); and

heating (see col. 4, lines 63-63-66) said substrate to cause said metal to react with said silicon in said first and said second drain regions and with said polysilicon of said first and second stacks to form a metal silicide (66) on said first drain, said second drain, and on said top polysilicon of said first and second stacks (see fig. 7).

With regards to the claimed sequence of method steps, e.g. forming the spacers after the formation of the drain regions, the court has held that selection of any order of performing process steps is *prima facie* obvious in the absence of new or unexpected results. *In re Burhans*, 154 F.2d 690, 69 USPQ 330 (CCPA 1946). Therefore, absent of unexpected results as in this case, is not considered inventive to change the sequence of steps.

Allowable Subject Matter

10. Claims 9-11 are allowed.

11. The following is a statement of reasons for the indication of allowable subject matter: the prior art fails to teach, disclose, or suggest, either alone or in combination, a method comprising the steps of: forming a trench between a first cell and a second cell; forming an opening in a first dielectric material in the trench; forming a shared source region through the opening; forming a second dielectric material in the opening; and forming sidewall spacers with the second dielectric material.

Response to Arguments

12. Applicant's arguments with respect to claims 4-11 have been considered but are moot in view of the new grounds of rejection.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Pio (US Pat. No. 6,127,224) discloses a memory cell with silicide contacts comprising spacers 31a-c (see abstract and figs. 2 and 17); Ma et al. (US Pat. No. 6,346,725 B1) discloses anisotropic etching sidewall spacers in figure 3D; and Chen et al. (US Pat. No. 6,017,796) discloses an EEPROM with silicide contact 326 and 324 in figure 7B.

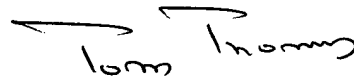
Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R. Díaz whose telephone number is (571) 272-1727. The examiner can normally be reached on Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, appearing to read "Tom Thomas", with a stylized flourish above the name.

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

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8/17/04